Remarks

Claims 2-4 and 6-8 are pending in the subject application. By this Amendment, claims 3 and 7 have been amended and claims 11 and 12 have been added. Upon entry of these amendments, claims 2-4, 6-8, and 11-12 will be before the Examiner. Favorable consideration of the pending claims is respectfully requested.

New claims 11 and 12 have been added. Support for new claim 11 can be found, at least, at Fig. 2C and paragraph [0012]. Support for new claim 12 can be found, at least at Fig. 2a and paragraph [0010]. No new matter has been introduced by these amendments.

Claims 2-4 and 6-8 are rejected under 35 USC §103(a) as being unpatentable over Prall *et al.* (U.S. 6,624,024) in view of Inrammanesh (U.S. 5,514,900). Applicants respectfully traverse. The Office Action at page 4 states that "Prall discloses in Fig. 5 a gap filling layer 50 at least substantially fills a gap," and that "the features upon which applicant relies (i.e., the undoped polysilicon or amorphous silicon is used to form the filling layer 24 without voids being created) are not recited in the rejected claim(s)." In order to further clarify that the narrow gaps between the gate areas are filled with the filling layer 24 without any voids, claims 3 and 7 have been amended accordingly to incorporate the feature of the gap filling layer being formed without voids using undoped polysilicon or amorphous silicon. Support for these amendments can be found at least at paragraphs [0010] and [0013]. No new matter has been introduced by these amendments.

In regards to the statement at page 4 of the Office Action that "as shown in Fig. 2b of the Applicant's specification, the gap filling layer 24 is a spacer form on sidewalls of the spacer," the gap filling layer 24 is a spacer form on sidewalls of the spacer at the non narrow gaps of Fig. 2b. However, the gap filling layer fills narrow gaps between adjacent gate areas without any voids. Prall *et al.* fails to teach or suggest filling a narrow gap between adjacent gate areas without any voids, wherein the gap filling layer remains in the narrow gap without being substantially removed by the anisotropic etching as specified in subject claims 2-4, 6-8, and 11-12.

Moreover, after performing the anisotropic etching, a part of the gap filling layer remains in the narrow gaps between adjacent gate areas while another part of the gap filling layer has been etched by the anisotropic etching to expose a surface of the substrate. This limitation is reflected in amended claim 7 and new claim 11. In contrast, Prall *et al.* teaches, at col. 5, lines 36-43 "[a]fter forming nitride spacers 48, a thin blanket etch resistant layer 50 . . . is formed according to

techniques known in the art. Layer **50** covers all exposed features, but in particular covers the exposed gate oxide **16**. Subsequently, a blanket planarized dielectric layer such as borophoshosilicate glass (BPSG) **52** is formed over the wafer surface." (Underline added). Applicants respectfully request reconsideration and withdrawal of the §103(a) rejection of claims 2-4 and 6-8.

In view of the foregoing remarks and amendments to the claims, Applicants believe that the currently pending claims are in condition for allowance, and such action is respectfully requested.

The Commissioner is hereby authorized to charge any fees under 37 C.F.R. §§ 1.16 or 1.17 as required by this paper to Deposit Account 19-0065.

The applicants invite the Examiner to call the undersigned if clarification is needed on any of this response, or if the Examiner believes a telephonic interview would expedite the prosecution of the subject application to completion.

Respectfully submitted,

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JL/sjk
Attachments: Request for Continued Examination including Petition and Fee for Extension of Time.